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Boosting the voltage gain of graphene FETs through a differential amplifier scheme with positive feedback

R. Grassi^{a,1,*}, A. Gnudi^a, V. Di Lecce^a, E. Gnani^a, S. Reggiani^a, G. Baccarani^a

^a*E. De Castro Advanced Research Center on Electronic Systems (ARCES), University of Bologna, Viale del Risorgimento 2, 40136 Bologna, Italy*

Abstract

We study a possible circuit solution to overcome the problem of low voltage gain of short-channel graphene FETs. The circuit consists of a fully differential amplifier with a load made of a cross-coupled transistor pair. Starting from the device characteristics obtained from self-consistent ballistic quantum transport simulations, we explore the circuit parameter space and evaluate the amplifier performance in terms of dc voltage gain and voltage gain bandwidth. We show that the dc gain can be effectively improved by the negative differential resistance provided by the cross-coupled pair. Contact resistance is the main obstacle to achieving gain bandwidth products in the terahertz range. Limitations of the proposed amplifier are identified with its poor linearity and relatively large Miller capacitance.

Keywords: Differential amplifier, gain enhancement, graphene FET, positive feedback, radio-frequency operation

1. Introduction

Graphene has received considerable interest in recent years for radio-frequency (RF) applications [1, 2]. Its high intrinsic carrier mobility [3] and large Fermi velocity [4] promise a high device transconductance g_m , which should in principle enable

*Corresponding author

Email addresses: rgrassi@arces.unibo.it (R. Grassi), agnudi@arces.unibo.it (A. Gnudi), vdilecce@arces.unibo.it (V. Di Lecce), egnani@arces.unibo.it (E. Gnani), sreggiani@arces.unibo.it (S. Reggiani), gbaccarani@arces.unibo.it (G. Baccarani)

¹Phone: +39 051 209 3772 ; Fax: +39 051 209 3779

device operation up to the terahertz range of frequencies. Integrated circuits made of graphene FETs (GFETs) have already been demonstrated [5, 6] and cut-off frequencies of hundreds of gigahertz, competing with the ones of III-V HEMTs, have indeed been reported [7–10]. Despite these progresses, challenges still remain, in particular, in achieving maximum oscillation frequencies comparable with cut-off frequencies for power amplifier applications [11, 12] and intrinsic gains g_m/g_d (g_d is the device drain conductance) suitable for voltage amplifier applications [11, 13–15]. The latter problem is due to the poor current saturation (i.e., large g_d) in monolayer GFETs related to the absence of a band gap [16, 17]. Values of voltage gain up to 14 have actually been reported for graphene inverters made of long-channel monolayer devices (of the order of $1\ \mu\text{m}$) [15, 18]. However, as the channel length is scaled down, the gain gets much worse [11] since velocity saturation due to carrier scattering, which helps current saturation, gets suppressed.

The use of bilayer graphene has been proven to effectively improve the gain of GFETs, leading to g_m/g_d values as high as 35 thanks to a band gap opening effect [19, 20]. However, this kind of device inherently requires large electric fields and large voltage drops in the vertical direction. In a recent paper of ours [21] we have investigated a different approach toward the improvement of the voltage gain, which relies on the effect of negative differential resistance (NDR) occurring in the output characteristics of monolayer devices under specific bias conditions. A gain enhancement can be obtained thanks to a cancellation effect between the negative g_d and the positive conductance of the load. The advantage over the bilayer GFET is that the presence of a back gate with a large applied voltage is not essential, although it can be useful in order to provide electrostatic doping of the source and drain access regions. On the other hand, the major drawback is represented by the difficulty in controlling circuit stability, which requires a proper compensation at both the input and the output ports and limits the scope of possible applications.

In the context of standard CMOS analog circuit design, a technique based on a similar concept of conductance cancellation (named “positive-feedback” or “negative conductance” technique) has been proposed to enhance the gain and gain-bandwidth-product (GBW) of amplifiers [22–24]. In this case, the output conductance is positive

and a feedback from the output node is used to generate a negative load conductance that compensates its value, thereby achieving high gains. Such technique could also be applied to GFET-based amplifiers. Since the devices would operate in the standard non-NDR regime, the aforementioned stability problems would be avoided. It is the purpose of this work to investigate such an idea, through a numerical study of the small-signal performance of a specific positive-feedback amplifier made by short-channel GFETs.

The paper is organized as follows. Section 2 deals with the reference GFET that is used as building block of the amplifier: the device structure, simulation model, and device characteristics are briefly discussed. In Section 3 the amplifier circuit is presented. Therein, a detailed circuit analysis, based on the simulated characteristics of the single device and focused on the amplifier dc gain and gain bandwidth, is reported. Conclusions are finally drawn in Section 4.

2. Structure, model, and simulation results of the intrinsic device

The device is identical to the one considered in our previous work [21]. The structure is a dual-gate GFET, with a top gate length of 20 nm (Fig. 1a). The top dielectric is a 1.2-nm-thick layer of Al_2O_3 (effective oxide thickness of 0.5 nm), whereas the back dielectric is silicon oxide with thickness of 10 nm. The back gate is used as a means to electrostatically dope the graphene access regions between the top gate and the source and drain contacts, and it could be replaced by a second top gate covering the access regions alone.

The dc characteristics of the device are computed with an in-house developed code for GFETs, based on the self-consistent solution of the 2-D Poisson equation and the ballistic non-equilibrium Green's function (NEGF) equations [25], with a p_z tight-binding Hamiltonian (more details can be found in [21]).

The small-signal frequency analysis is based on a small-signal equivalent circuit (see [21, Fig. 2]) whose intrinsic part is derived from [26]. The intrinsic small-signal circuit parameters are extracted from the simulated dc I - V and Q - V characteristics using finite differences. As for the parasitics, we consider the possibility of non-zero source and drain contact resistances; sensitivity to gate resistance and parasitic capaci-

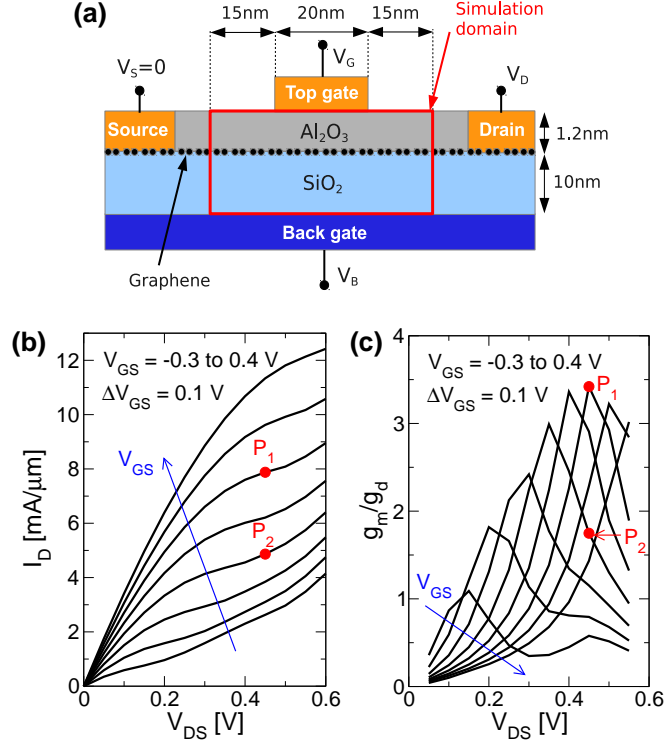


Figure 1: (a) Longitudinal cross-section of the simulated GFET. (b) Output characteristics at $V_{BS} = 9$ V showing n-type-FET operation. (c) Corresponding intrinsic voltage gain. A zero top-gate/graphene workfunction difference Φ_{mg} is assumed. P_1 and P_2 are specific operating points. Figs. (a–b) are adapted from [21].

tances is considered for one specific case.

Fig. 1b shows the device output characteristics obtained with a back-gate-to-source voltage $V_{BS} = 9$ V and assuming a zero metal-graphene workfunction difference for both gates (in this paper the back-gate/graphene workfunction difference will always be taken to be zero). Such value of V_{BS} corresponds to a heavy n-type doping of the source and drain regions. In all the range of top-gate-to-source voltage V_{GS} considered in the plot, the channel doping is also n-type and the device operates as a conventional n-type FET, although showing only a weak (or “quasi-”) saturation. The resulting intrinsic gain is limited to about 3.4 (Fig. 1c). Thanks to the symmetry of the graphene bandstructure and the use of an electrostatic doping, the same device exhibits p-type

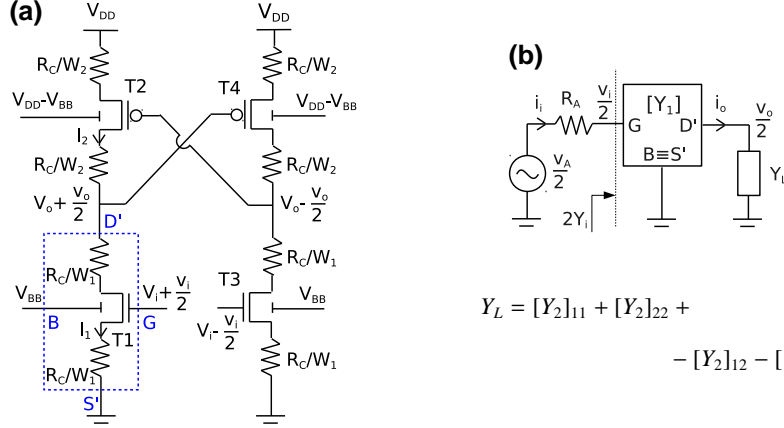


Figure 2: (a) Schematic of the CS differential amplifier. Transistors T1 and T2 are identical to T3 and T4, respectively. Resistors represent source and drain contact resistances. (b) Corresponding small-signal model, where $[Y_1]$ ($[Y_2]$) is the Y-matrix of the extrinsic transistor T1 (T2). Y_L is calculated from $[Y_2]$ as indicated. R_A is the output resistance of the input voltage source.

characteristics completely symmetrical to the ones in Fig. 1b if the polarities of all voltages, including V_{BS} , are reversed (not shown).

3. Analysis of the “positive-feedback” amplifier

The amplifier circuit considered here (Fig. 2a) is similar to the first one proposed in the literature on positive-feedback amplifiers (see [23, Fig. 1a]). It is a common-source (CS) fully differential amplifier with n-type driver transistors and an active load made of cross-coupled p-type transistors. Although different symbols are used in Fig. 2a to indicate n- and p-type transistors, they actually share the same structure: as explained in Section 2, one or the other type of transistor is obtained by changing the polarity of V_{BS} . The circuit is symmetric, in the sense that transistors T1 and T2 are respectively identical to T3 and T4. On the other hand, T1 and T2 may have different channel widths (W_1 and W_2 , respectively) or different top gate materials, resulting in different top-gate/graphene workfunction differences (Φ_{mg1} and Φ_{mg2} , respectively, with Φ_{mg1} assumed zero). Contact resistances are treated as fixed parameters independent of bias. We consider a common value for the source and drain contact resistances of the same transistor (because of the symmetry of the device structure), and we assume it to scale

with the inverse of the channel width ($1/R_C$ is the contact conductance per unit width). Unprimed/primed symbols are used to indicate intrinsic/extrinsic device terminals, as done in Fig. 2a for T1 (the blue box represents the “extrinsic” device T1). The circuit equations are solved using a spline interpolation of the device I – V characteristics obtained in Section 2.

Thanks to the symmetry of the amplifier, a simple small-signal equivalent circuit is derived for the case of purely differential (zero common mode) signals (Fig. 2b), which involves only the Y -matrices of transistors T1 and T2 ($[Y_1]$ and $[Y_2]$, respectively), which, in turn, are easily calculated from the device small-signal equivalent circuit.

According to the symbol definitions in Fig. 2b, the amplifier voltage gain is given by $A_v = v_o/v_i = -[Y_1]_{21}/([Y_1]_{22} + Y_L)$ and takes a simple form at frequency $f = 0$:

$$A_{v0} = -\frac{\tilde{g}_{m1}}{\tilde{g}_{d1} + \tilde{g}_{d2} - \tilde{g}_{m2}}, \quad (1)$$

where $g_{m1}/\tilde{g}_{m1} = g_{d1}/\tilde{g}_{d1} = [1 + (R_C/W_1)(2g_{d1} + g_{m1} + g_{mb1})]$, with g_{d1} , g_{m1} , and g_{mb1} the drain conductance, top-gate transconductance, and back-gate transconductance of T1, respectively (similar definitions hold for T2). Eq. 1 explains the gain-enhancement effect: the term $G_L = \tilde{g}_{d2} - \tilde{g}_{m2}$, which is the load conductance due to T2, can be negative and compensate \tilde{g}_{d1} . The gain is theoretically infinite if the matching is exact. However, the circuit becomes unstable for $\tilde{g}_{d1} + G_L < 0$ (or $A_{v0} > 0$)². If conventional well-saturated MOSFETs were used, $g_m \gg g_d$, hence additional diode-connected transistors in parallel to the cross-coupled load transistors would be required to allow circuit stability [23, Fig. 1a]. These are not necessary in our GFET implementation since $g_m \sim g_d$ (Fig. 1c).

3.1. Dc voltage gain and voltage gain bandwidth

The circuit operating point is determined by a considerable numbers of variables/parameters, e.g., V_i , V_{BB} , V_{DD} , W_2/W_1 , Φ_{mg2} and R_C (see Fig. 2a; W_1 can be taken as the

²We are referring here to the stability of the amplifier connected to a short circuit at the input port and to an open circuit at the output port. The stability in other source/load conditions can be evaluated with the standard stability-circle technique [27].

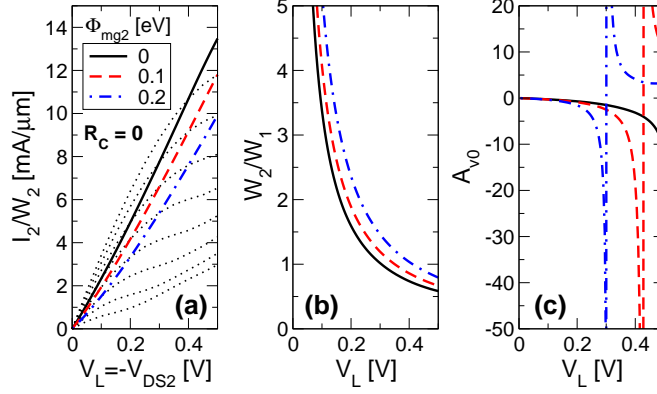


Figure 3: Analysis of the dc voltage gain as a function of $V_L = V_{DD} - V_o$. The operating point of T1 is held constant at P_1 and a zero contact resistance is assumed. (a) I - V characteristics of diode-connected T2 for different values of top-gate/graphene workfunction difference Φ_{mg2} . The dotted lines show the T2 output characteristics at constant $V_{GS2} + \Phi_{mg2}$ from -0.4 V (top curve) to 0.3 V (bottom curve) in steps of 0.1 V. (b) Corresponding ratio between the widths of T1 and T2, which is determined by the constraint $I_1 = I_2$. (c) Corresponding dc voltage gain. Positive values indicate an unstable circuit.

reference width). In order to simplify the analysis, we choose to fix the operating point of T1, for example, at the point P_1 of maximum g_m/g_d of Figs. 1b–c, which, according to (1), should favor high amplifier gains since it also corresponds to high g_m ($\simeq 17$ mS/ μ m). In this way, for a given value of R_C , we fix V_i , V_{BB} , as well as the output voltage V_o and the current I_1 that flows through T1. For a given value of Φ_{mg2} , a relation between V_{DD} (or $V_L = V_{DD} - V_o$) and W_2 is obtained from the I - V characteristics of T2 and the constraint $I_2 = I_1$.

The above procedure is illustrated in Fig. 3, where we take the bias point of T1 equal to P_1 , $R_C = 0$, and we consider three values of Φ_{mg2} . For each value of V_{DD} , we first compute the current per unit width through T2, I_2/W_2 , by imposing its top-gate and drain voltages to be equal (Fig. 3a). Then, we calculate W_2/W_1 from $W_2/W_1 = (I_1/W_1)/(I_2/W_2)$ (Fig. 3b). Finally, having set the operating points of both T1 and T2, we obtain the amplifier gain A_{v0} using (1) (Fig. 3c). It can be observed that, if $\Phi_{mg2} = 0$ and V_L is limited to 0.5 V, the maximum gain is only 12, which means that G_L is not sufficiently negative. In order to further decrease G_L , which is reduced to $G_L = g_{d2} - g_{m2}$ in the case of $R_C = 0$, one needs to increase the ratio g_{m2}/g_{d2} , i.e., to

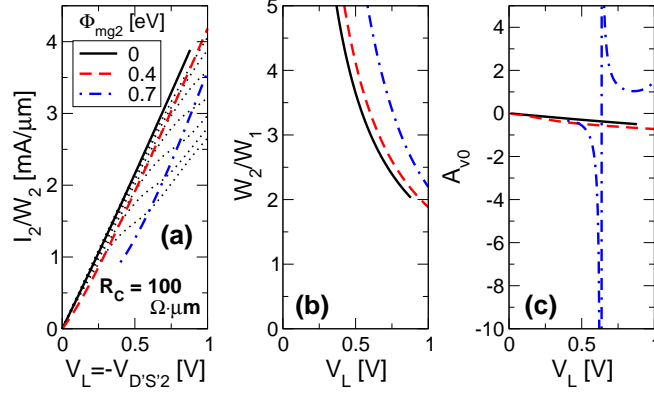


Figure 4: Same as in Fig. 3 but for $R_C = 100 \Omega \cdot \mu\text{m}$. Here, $V_{BB} = 9.79 \text{ V}$. The dotted lines in (a) are the output characteristics of the extrinsic transistor T2 at constant $V_{GS'2} + \Phi_{mg2}$ from -0.5 V (top curve) to 0.1 V (bottom curve) in steps of 0.1 V .

move the operating point of T2 into the quasi-saturation region. This can be achieved by choosing a suitable top-gate material of T2 that provides $\Phi_{mg2} > 0$, as shown in Fig. 3a, where the T2 output characteristics at constant $V_{GS'2} + \Phi_{mg2}$ are also shown for comparison. The considered values of Φ_{mg2} are within the range of workfunction of several metals [28]. Increasing Φ_{mg2} also leads to the aforementioned divergence and change of sign of A_{v0} , which mark the beginning of the instability region (Fig. 3c). It should be noted that the resulting values of W_2/W_1 are reasonable in all three cases.

The same procedure has been repeated for the case of $R_C = 100 \Omega \cdot \mu\text{m}$ (Fig. 4), a value which is within reach of present graphene technology [29]. It is seen that, given a maximum V_L voltage of 1 V , it is still possible to achieve high gains, but a larger Φ_{mg2} is required to move the bias point of T2 into the quasi-saturation region ($\Phi_{mg2} \approx 0.7 \text{ eV}$ could be achieved with, for example, Au, Pd, or Pt [28]).

The amplifier bandwidth is evaluated by numerically computing the frequency f_p of the dominant pole of $A_v(s) = v_o(s)/v_i(s)$. In the case of $R_C = 0$, an analytical expression is available:

$$f_p = \frac{1}{2\pi} \frac{g_{d1} + g_{d2} - g_{m2}}{C_{dd1} + C_L}, \quad (2)$$

where $C_L = C_{gg2} + C_{dd2} + C_{gd2} + C_{dg2}$ (the subscripts “1” and “2” refer respectively to T1 and T2 as usual), and the capacitances are defined as $C_{kk} = \partial Q_K / \partial V_K$ and $C_{kl}|_{k \neq l} =$

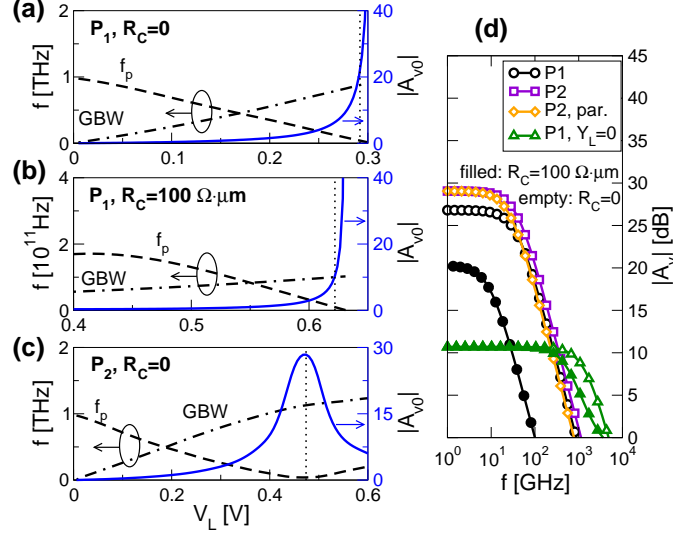


Figure 5: (a–c) Dc voltage gain, dominant pole frequency, and gain bandwidth product vs. V_L for different operating points of T1 and values of contact resistance (see legend). Values of Φ_{mg2} in (a–c) are 0.2, 0.7, and 0.2 eV, respectively. (d) Frequency magnitude response of voltage gain at the V_L points indicated by vertical dotted lines in (a–c). The performance of transistor T1 with open circuit load ($Y_L = 0$) is also shown for comparison. The curve labeled “P2, par.” is obtained at the operating point P_2 including gate resistance and parasitic capacitances as described in the text.

$-\partial Q_K / \partial V_L$ ($k, l \in \{g, d, s, b\}$), with the charges Q_K computed as described in [21]. The gain-bandwidth-product is defined as $\text{GBW} = |A_{v0}|f_p$.

The plots of f_p and GBW for the cases of $R_C = 0$ and $\Phi_{mg2} = 0.2$ eV and of $R_C = 100 \Omega \cdot \mu\text{m}$ and $\Phi_{mg2} = 0.7$ eV are shown in Figs. 5a–b, respectively, where we also replot the respective dc gain from Figs. 3–4. Contact resistance has a dramatic effect on both f_p and GBW, reducing them by almost one order of magnitude.

It is interesting to see how the RF performance is affected by choosing a different bias point for T1, for example, the point P_2 of Figs. 1b–c, which corresponds to a lower g_m ($\approx 11.9 \text{ mS}/\mu\text{m}$). As shown in Fig. 5c for the case of $R_C = 0$, the performance is actually improved. Higher values of GBW (exceeding 1 THz) can be achieved, which means that the lower g_m gets compensated by smaller capacitances. In addition, the dc gain is bounded, which indicates that the circuit is stable over the whole considered range of V_L .

Table 1: RF metrics from Fig. 5d.

	$R_C = 0 \, \Omega \cdot \mu\text{m}$				$R_C = 100 \, \Omega \cdot \mu\text{m}$	
	P_1	P_2	P_2 , par.	P_1 , $Y_L = 0$	P_1	$P_1, Y_L = 0$
$ A_{v0} $	21.9	28.4	28.4	3.42	10.3	3.42
f_p [GHz]	40.1	39.8	27.4	1460	9.7	585
GBW [GHz]	878	1130	777	4990	100	2000

The frequency magnitude response of A_v for the three cases in Figs. 5a–c and at specific V_L points is shown in Fig. 5d. There, we also include the voltage gain that one would obtain without recurring to positive feedback, i.e., of transistor T1 with open circuit load ($Y_L \equiv 0$). Moreover, we include the results obtained by repeating one of the simulations with non-zero gate resistance R_g and non-zero parasitic capacitances C_{int} and C_{ext} between intrinsic and extrinsic gate and source and drain terminals, respectively. The values of the parasitics of T1 have been taken equal to the ones in [21] ($R_g = 4 \, \Omega$ and $C_{int} = C_{ext} = 0.1$ fF), which were estimated for a channel width $W = 1 \, \mu\text{m}$. The values of the parasitics of T2 have been fixed accordingly, assuming the scaling relations $R_g, C_{int}, C_{ext} \propto W$.

The figures of merit extracted in the different cases are reported in Table 1. It is seen that the load admittance introduced by the positive feedback significantly degrades GBW and also increases the sensitivity of GBW to contact resistance. The effect of gate resistance and parasitic capacitances is not as drastic as contact resistance since the corresponding degradation of GBW is only 31%.

It is worth noting that, in all three cases considered in Figs. 5a–c, the qualitative trends of f_p and GBW with respect to V_L are similar: f_p decreases with increasing $|A_{v0}|$, whereas GBW monotonically increases with V_L . This can be understood, at least in the case of $R_C = 0$, with the help of (1) and (2). Combining them, one obtains $f_p \propto |A_{v0}|^{-1}(C_{dd1} + C_L)^{-1}$, which implies $\text{GBW} \propto (C_{dd1} + C_L)^{-1}$. According to the latter expression, since GBW is found to increase with V_L , the capacitance C_L related to T2 must correspondingly decrease. This is confirmed by the analysis of the various

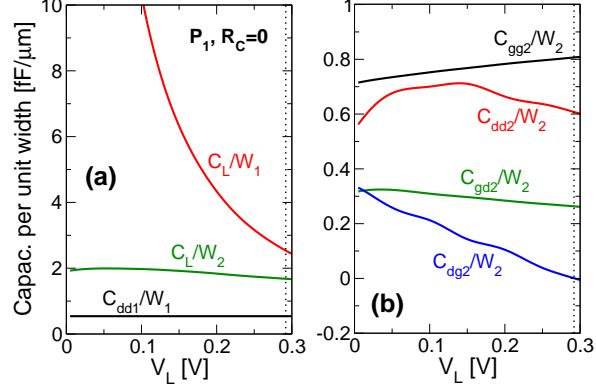


Figure 6: Small-signal capacitances for the case considered in Fig. 5a. (a) Dependence on V_L of C_{dd1} and C_L , which contribute to f_p according to Eq. 2. (b) Dependence on V_L of the different contributions to C_L . The vertical dotted lines are located as in Fig. 5a.

capacitances in Fig. 6, where we have considered the case of bias point P_1 and $R_C = 0$. The change in C_L/W_1 with respect to V_L is caused by both the change of operating point of T2 and the adjustment of the ratio W_2/W_1 (recall Figs. 3a–b). Comparing C_L/W_1 with C_L/W_2 , which, on the contrary, is independent of W_2/W_1 , it is clear that the latter cause is predominant.

3.2. Low-voltage operation

The strategy followed so far to find the optimal bias point of the amplifier, which consists in keeping the operating point of T1 fixed and moving V_L , uses V_{DD} as a freely adjustable parameter. For example, a value of $V_{DD} \simeq 0.92$ V is required to bias the amplifier in the point of maximum gain of Fig. 5c. In order to verify if the proposed circuit can work at lower supply voltage, we have solved the circuit equations for a fixed $V_{DD} = 0.55$ V, sweeping the input voltage V_i for different W_2/W_1 ratios. The results are shown in Fig. 7. It is seen that, at least if $R_C = 0$, it is still possible to find a bias point which provides at the same time both high gain (> 10) and GBW above 1 THz.

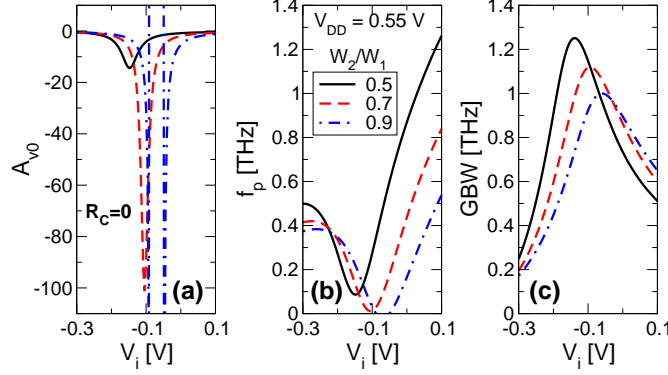


Figure 7: Dc voltage gain (a), dominant pole frequency (b), and gain bandwidth product (c) as a function of V_i . Here the supply voltage is held constant at 0.55 V and three different values of W_2/W_1 are considered. A zero contact resistance is assumed. The other parameters are: $V_{BB} = 9$ V and $\Phi_{mg2} = 0.3$ V.

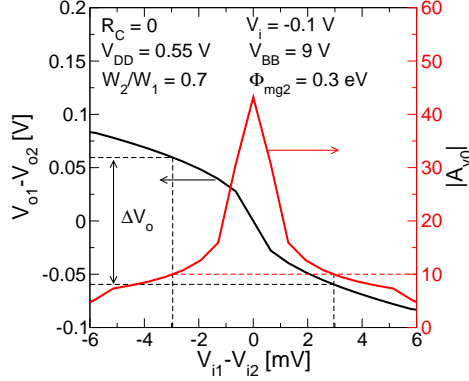


Figure 8: Differential voltage transfer characteristics and corresponding voltage gain obtained with the parameters indicated in the legend. The common-mode input voltage is chosen close to the point of maximum gain of the curve with $W_2/W_1 = 0.7$ in Fig. 7a. ΔV_o is defined in the text.

3.3. Non-linearity

Let V_{i1} and V_{i2} be the voltages applied to the gates of T1 and T3, respectively, which are reduced to $V_i + v_i/2$ and $V_i - v_i/2$ in the case of a small purely differential signal (Fig. 2a). The strong dependence of A_{v0} on V_L and V_i shown in Figs. 3–5 and 7 indicates a strong non-linearity. We have verified this by computing the differential voltage transfer characteristics for the case in Fig. 7 with $W_2/W_1 = 0.7$ and a value of $V_i = -0.1$ V close to the point of maximum gain. As shown in Fig. 8, the strong

sensitivity of the gain to the input voltage results in a small high-gain output voltage range ΔV_o compared to V_{DD} : for example, defining ΔV_o as the output voltage range where $|A_{v0}| > 10$, we have $\Delta V_o/V_{DD} \simeq 0.22$. The problem is inherently related to the compensation technique and it was also found to affect NDR GFETs [21]. In the literature on positive-feedback amplifiers, some more complex versions of the amplifier have been proposed to reduce non-linearity [23].

3.4. Miller effect

Thus far, we have not taken into account the output resistance R_A of the input voltage source (see circuit of Fig. 2b). If R_A is not sufficiently small, the bandwidth of the total voltage gain v_o/v_A can be limited by the bandwidth of $v_i/v_A = (1 + 2R_A Y_i)^{-1}$, which depends on the amplifier input admittance Y_i (the symbols are defined in Fig. 2b). In the case of $R_C = 0$, it can be shown that, at low frequency, Y_i takes the form:

$$Y_i(s) \sim sC_i, \quad C_i = (C_{gg1} + C_{gd1}|A_{v0}|)/2. \quad (3)$$

Contrary to traditional MOSFETs, where C_{gd} is only due to conventional electrostatic drain-induced barrier lowering, a pronounced drain quantum capacitance arising from the lack of a band gap also contributes to C_{gd} in GFETs [30]. For example, $C_{gd1}/C_{gg1} \simeq 0.39$ at the operating point P_2 (the values per unit width of the two capacitances are similar to those shown in Fig. 6b for T2). The expression in (3), although valid only at low frequency, suggests that a high dc gain $|A_{v0}|$ might have a negative impact on the bandwidth of v_o/v_A through a large Y_i . This is the well-known Miller effect, which is typical of CS amplifiers. The real and imaginary parts of the normalized Y_i are shown in Fig. 9a for the case in Fig. 5c with $V_L = 0.474$ V. It is seen that the approximation in (3) represents a good fit of Y_i up to about 10 GHz. To evaluate the impact of $\Im\{Y_i\}$ on the amplifier bandwidth, we numerically compute the -3 dB frequency of v_o/v_A as a function of R_A (Fig. 9b). The bandwidth drops already at $R_A W_1 \sim 100 \Omega \cdot \mu\text{m}$, indicating that the input susceptance is relatively large.

3.5. Common-gate variant

Since Miller's effect is usually mitigated in the common-gate (CG) configuration, we have considered a CG version of the amplifier (the input transistor connection is

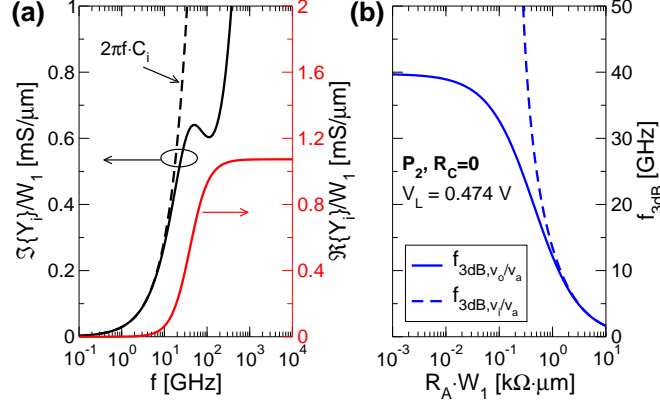


Figure 9: (a) Real and imaginary parts of the input admittance Y_i as a function of frequency (solid lines) for the case considered in Fig. 5c with $V_L = 0.474$ V. The dashed line is the plot of $2\pi f C_i$ with $C_i = 4.7$ fF/ μm . (b) -3dB frequency of voltage gains v_o/v_A and v_i/v_A as a function of the source resistance R_A (see Fig. 2b for the definitions).

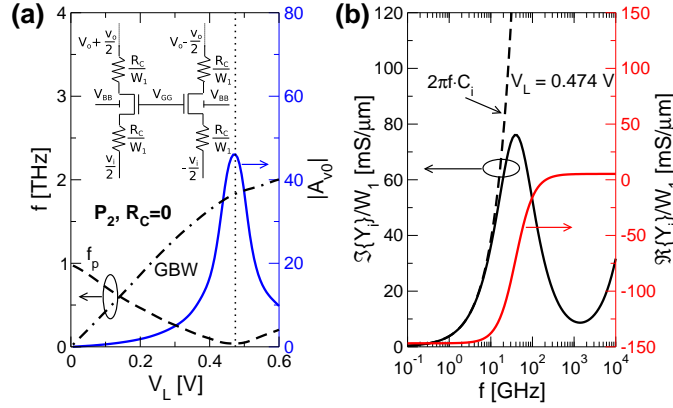


Figure 10: (a) Same as in Fig. 5c but for the CG configuration (the input transistor connection is shown in the inset). The RF metrics at $V_L = 0.474$ V are: $|A_{v0}| = 46.1$, $f_p = 39.8$ GHz, and $\text{GBW} = 1.83$ THz. (b) Same as in Fig. 9a but for the CG configuration. Here, $C_i = 610$ fF/ μm .

shown in the inset of Fig. 10a, whereas the cross-coupled load transistors are identical to the CS case) and repeated the analysis of the RF performance with varying V_L at a fixed operating point of T1, using the same parameters as in Fig. 5c. The results in Fig. 10a show that the CG amplifier has identical f_p and slightly higher A_{v0} and GBW compared to the CS amplifier. Indeed, in the CG configuration and in the case

of $R_C = 0$, the dc gain is given by $A_{v0} = (g_{m1} + g_{mb1} + g_{d1})/(g_{d1} + g_{d2} - g_{m2})$, which differs from the CS expression because of the additional term $g_{mb1} + g_{d1} \sim g_{d1}$ in the numerator. Unfortunately, the CG amplifier is not unilateral at low frequency due to the high value of g_d between the input and output ports. Looking at the plot of the real part of Y_i in Fig. 10b, it is clear that the negative load conductance gives rise to a negative input conductance. Indeed, it can be shown that $Y_i|_{f=0} = A_{v0}G_L$. Because of the negative $\Re\{Y_i\}$ at low frequency, the circuit is unstable for $R_A W_1 > 6.8 \Omega \cdot \mu\text{m}$. Notwithstanding the $\Im\{Y_i\}$ values, the CG configuration is thus ruled out.

4. Conclusions

In this work, we have investigated the use of the positive-feedback technique to increase the voltage gain of GFET-based amplifiers in CS configuration. The RF performance of the reference amplifier has been evaluated through a small-signal analysis with parameters extracted from atomistic quantum transport simulations. The analysis has shown that, with a proper choice of the relative widths of the transistors and of the gate metal workfunctions, it is possible to find bias points with high dc gain (> 10), even at relatively small supply voltages. On the other hand, the dc gain is strongly sensitive to the bias point, a problem which is common to other conductance compensation techniques. Contact resistance at typical experimental values has been found to significantly degrade GBW, which would be otherwise in the terahertz range. The amplifier bandwidth can also be negatively affected by Miller's effect, if the output resistance of the input voltage source is not sufficiently small. The use of the CG configuration to circumvent the Miller effect is ruled out due to stability problems.

Acknowledgments

This work has been supported by the EU project GRADE 317839.

References

References

- [1] F. Schwierz, Graphene transistors, *Nature Nanotechnology* 5 (7) (2010) 487–496.

- [2] F. Schwierz, Graphene Transistors: Status, Prospects, and Problems, *Proceedings of the IEEE* 101 (7) (2013) 1567–1584.
- [3] K. I. Bolotin, K. J. Sikes, Z. Jiang, M. Klima, G. Fudenberg, J. Hone, P. Kim, H. L. Stormer, Ultrahigh electron mobility in suspended graphene, *Solid State Communications* 146 (9–10) (2008) 351–355.
- [4] A. K. Geim, K. S. Novoselov, The rise of graphene, *Nature Materials* 6 (3) (2007) 183–191.
- [5] H. Wang, A. Hsu, J. Wu, J. Kong, T. Palacios, Graphene-Based Ambipolar RF Mixers, *IEEE Electron Device Letters* 31 (9) (2010) 906–908.
- [6] Y.-M. Lin, A. Valdes-Garcia, S.-J. Han, D. B. Farmer, I. Meric, Y. Sun, Y. Wu, C. Dimitrakopoulos, A. Grill, P. Avouris, K. A. Jenkins, Wafer-scale graphene integrated circuit, *Science* 332 (6035) (2011) 1294–1297.
- [7] L. Liao, Y.-C. Lin, M. Bao, R. Cheng, J. Bai, Y. Liu, Y. Qu, K. L. Wang, Y. Huang, X. Duan, High-speed graphene transistors with a self-aligned nanowire gate, *Nature* 467 (7313) (2010) 305–308.
- [8] Y.-M. Lin, C. Dimitrakopoulos, K. A. Jenkins, D. B. Farmer, H.-Y. Chiu, A. Grill, P. Avouris, 100-GHz Transistors from Wafer-Scale Epitaxial Graphene, *Science* 327 (5966) (2010) 662.
- [9] Y. Wu, Y.-M. Lin, A. A. Bol, K. A. Jenkins, F. Xia, D. B. Farmer, Y. Zhu, P. Avouris, High-frequency, scaled graphene transistors on diamond-like carbon, *Nature* 472 (7341) (2011) 74–78.
- [10] R. Cheng, J. Bai, L. Liao, H. Zhou, Y. Chen, L. Liu, Y.-C. Lin, S. Jiang, Y. Huang, X. Duan, High-frequency self-aligned graphene transistors with transferred gate stacks, *Proceedings of the National Academy of Sciences* 109 (29) (2012) 11588–11592.
- [11] Y. Wu, K. A. Jenkins, A. Valdes-Garcia, D. B. Farmer, Y. Zhu, A. A. Bol, C. Dimitrakopoulos, W. Zhu, F. Xia, P. Avouris, Y.-M. Lin, State-of-the-art graphene high-frequency electronics, *Nano Letters* 12 (6) (2012) 3062–3067.

- [12] Z. Guo, R. Dong, P. S. Chakraborty, N. Lourenco, J. Palmer, Y. Hu, M. Ruan, J. Hankinson, J. Kunc, J. D. Cressler, C. Berger, W. A. de Heer, Record maximum oscillation frequency in C-face epitaxial graphene transistors, *Nano Letters* 13 (3) (2013) 942–947.
- [13] S.-J. Han, K. A. Jenkins, A. Valdes Garcia, A. D. Franklin, A. A. Bol, W. Haensch, High-frequency graphene voltage amplifier, *Nano Letters* 11 (9) (2011) 3690–3693.
- [14] E. Guerriero, L. Polloni, L. G. Rizzi, M. Bianchi, G. Mondello, R. Sordan, Graphene audio voltage amplifier, *Small* 8 (3) (2012) 357–361.
- [15] L. G. Rizzi, M. Bianchi, A. Behnam, E. Carrion, E. Guerriero, L. Polloni, E. Pop, R. Sordan, Cascading wafer-scale integrated graphene complementary inverters under ambient conditions, *Nano Letters* 12 (8) (2012) 3948–3953.
- [16] I. Meric, M. Y. Han, A. F. Young, B. Ozyilmaz, P. Kim, K. L. Shepard, Current saturation in zero-bandgap, top-gated graphene field-effect transistors, *Nature Nanotechnology* 3 (2008) 654–659.
- [17] S.-J. Han, D. Reddy, G. D. Carpenter, A. D. Franklin, K. A. Jenkins, Current saturation in submicrometer graphene transistors with thin gate dielectric: Experiment, simulation, and theory, *ACS Nano* 6 (6) (2012) 5220–5226.
- [18] D. Schall, M. Otto, D. Neumaier, H. Kurz, Integrated ring oscillators based on high-performance graphene inverters, *Scientific Reports* 3 (2013) 2592.
- [19] B. N. Szafrank, G. Fiori, D. Schall, D. Neumaier, H. Kurz, Current Saturation and Voltage Gain in Bilayer Graphene Field Effect Transistors, *Nano Letters* 12 (3) (2012) 1324–1328.
- [20] G. Fiori, G. Iannaccone, Insights on radio frequency bilayer graphene FETs, in: *IEEE International Electron Devices Meeting (IEDM)*, 2012, 2012, pp. 17.3.1–17.3.4.

- [21] R. Grassi, A. Gnudi, V. Di Lecce, E. Gnani, S. Reggiani, G. Baccarani, Exploiting negative differential resistance in monolayer graphene FETs for high voltage gains, *IEEE Transactions on Electron Devices* 61 (2) (2014) 617–624.
- [22] D. J. Allstot, A precision variable-supply CMOS comparator, *IEEE Journal of Solid-State Circuits* 17 (6) (1982) 1080–1087.
- [23] M. M. Amourah, R. L. Geiger, All digital transistor high gain operational amplifier using positive feedback technique, in: *IEEE International Symposium on Circuits and Systems, 2002. ISCAS 2002.*, Vol. 1, 2002, pp. I–701–I–704.
- [24] P. T. Tran, H. L. Hess, K. V. Noren, Operational amplifier design with gain-enhancement differential amplifier, in: *IECON 2012 - 38th Annual Conference on IEEE Industrial Electronics Society*, 2012, pp. 6248–6253.
- [25] S. Datta, *Quantum Transport: Atom to Transistor*, Cambridge University Press, Cambridge, UK, 2005.
- [26] Y. Tsividis, *Operation and modeling of the MOS transistor*, 2nd Edition, McGraw-Hill, Boston, MA, 1999.
- [27] D. M. Pozar, *Microwave engineering*, 3rd Edition, Wiley, Hoboken, NJ, 2005.
- [28] W. M. Haynes (Ed.), *CRC Handbook of Chemistry and Physics*, 94th Edition, CRC Press, 2013.
- [29] J. S. Moon, M. Antcliffe, H. C. Seo, D. Curtis, S. Lin, A. Schmitz, I. Milosavljevic, A. A. Kiselev, R. S. Ross, D. K. Gaskill, P. M. Campbell, R. C. Fitch, K.-M. Lee, P. Asbeck, Ultra-low resistance ohmic contacts in graphene field effect transistors, *Applied Physics Letters* 100 (20) (2012) 203512.
- [30] K. D. Holland, N. Paydavosi, N. Neophytou, D. Kienle, M. Vaidyanathan, RF Performance Limits and Operating Physics Arising From the Lack of a Bandgap in Graphene Transistors, *IEEE Transactions on Nanotechnology* 12 (4) (2013) 566–577.